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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/211,718	12/14/1998	ERIC R. FOSSUM	08305/015001	9540

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EXAMINER	
GENCO, BRIAN C	
ART UNIT	PAPER NUMBER
2615	15

DATE MAILED: 03/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/211,718	FOSSUM ET AL.	
	Examiner	Art Unit	
	Brian C Genco	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-12 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

The proposed drawing corrections and the proposed substitute sheets of drawings, filed on February 10, 2003 have been accepted.

Applicant's amendment filed February 10, 2003 has overcome the 35 U.S.C. 103(a) rejection of claims 1-7. Further, applicant's traversal of claim 8 has overcome the 35 U.S.C. 103(a) rejection of claim 8. Namely, examiner succeeds that neither Kawahara nor Stettner disclose correction of missing data due to gaps between butted image sensors, and while Sayag does disclose correction of missing data for the central readout register it would not have been obvious to one of ordinary skill in the art to extend that teaching to correct for missing data around the periphery of butted image sensors. Further, examiner succeeds that it would not have been obvious to on of ordinary skill in the art to butt Sayag's image sensor since it doesn't take on a rectangular shape. One would have to create an octagon with all the sides being equal length in order to successfully butt image sensors into a full format array. However, during refining of examiners search more pertinent prior art has been found.

Priority

Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, the provisional application upon which priority is claimed fails to provide adequate support under 35 U.S.C. 112 for claims 1-12 of this application. Examiner notes that provisional application number 60/069700 does not disclose a pixel interpolator located between said image area and said fourth edge. Examiner note in lines 13-14 applicant discloses that pixel interpolation be done in software. Further on lines 19-22 examiner notes that applicant discloses on-chip timing and control system, wherein on-chip pixel interpolation would not be enabled by an on-chip control system.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,886,353 to Spivey et al) in view of (USPN 5,510,623 to Sayag et al) in further view of (USPN 5,937,027 to Thevenin et al) in still further view of (USPN 6,396,539 to Heller et al).

In regards to claim 1 Spivey et al, herein Spivey, discloses a CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of rows and columns, and image sensor logic on said substrate, said logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor other than rows individually (e.g., column 4, line 57 – column 5, line 1; Fig. 15A; column 11, line 63 – column 12, line 5; column 12, lines 50-52; note that the chip logic associated with parts of said image sensor other than rows individually is readout circuit 133),

a substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge (e.g., Fig. 15A),

said image sensor extending between said first edge, said second edge, and said third edge, such that a first area adjacent said first edge of the chip includes first pixels of the image sensor, a second area adjacent said second edge of the chip includes image sensors, and a third area adjacent said third edge of the chip includes image sensors (e.g., column 26, lines 33-52;

note that if the readout circuitry is integrated with the pixel array then there would be image sensors adjacent the first, second, and third edges),

said row logic being physically located inside said image sensor (e.g., column 26, lines 33-52)

chip driver circuitry located between said image area and said fourth edge (e.g., Fig. 15A)

a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate (e.g., Figs. 17A, 19, and 20A)

Spivey does not disclose that said row logic be in place of a plurality of pixels of the array or a pixel interpolator between said image are and said fourth edge.

It is known in the art to place row logic inside said image sensor in place of a plurality of pixels as taught by Thevenin et al, herein Thevenin, and Sayag et al, herein Sayag. Thevenin discloses an invention for monitoring the exposure so as to maximize the image quality and minimize the dose of x-rays to an object of an x-ray imager by using two two-pixel-wide measurement areas (e.g., Fig. 3B; column 6, lines 42-61; column 7, lines 12-21; column 8, lines 21-27). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have used exposure monitoring in the x-ray imager of Spivey in order to optimize "exposure time of the object to ... radiation so as to produce at each taking of an image, an image of good quality while minimizing the dose of radiation to which the object is subjected (column 1, lines 9-12, Thevenin)." Sayag discloses the use of a centrally disposed read-out register that is photosensitive in order to monitor exposure (column 6, lines 57 – column 7, line 8; column 7, lines 29-32). This would be a preferred method of monitoring exposure since only

one two-pixel-wide measuring area would be used and thus less correction of missing pixels would be needed. Further, this would be preferred since the readout circuits are photosensitive one would gain the benefit of both exposure monitoring as taught by Thevenin and having the readout circuit in the interior of the image sensor so as to enable better butting of image sensors so as to form a large format array. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have had a centrally disposed photosensitive readout register so as to monitor x-ray exposure in order to maximize image quality while minimizing radiation dose as well as enabling butting of multiple arrays so as to form a large format array.

Assuming arguendo for combining the Sayag reference since the Sayag reference deals with a CCD image sensor an the other references deal with CMOS image sensors, examiner notes that it is very well known and established in the art that CCD and CMOS image sensors are analogous art and that CMOS image sensors are preferable since they cost less to manufacture. Official notice is taken. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have made Sayag's invention using CMOS image sensor technologies in order to reduce cost.

It is also known in the art to use on-chip pixel interpolation as taught by Heller et al, herein Heller. Heller discloses having an on-chip memory and controller unit for storing defective pixel locations so that the controller can interpolate values for the defective pixels from the surrounding pixels (e.g., column 8, lines 39-65; column 4, lines 5-9). Note that Heller discloses that it is preferable to include as much circuitry on-chip in order to reduce cost (column 1, line 56 – column 2, line 36). While Spivey and Thevenin both disclose using pixel interpolation this process is done off-chip, therefore it would have been obvious to one of

ordinary skill in the art at the time of the invention to have preformed pixel interpolation on-chip in order to reduce cost. Furthermore it would have been obvious to one of ordinary skill in the art at the time of the invention to have place the pixel interpolator between said image area and said fourth edge so as to still enable butting for the creation of a large format array as taught by Spivey.

In regards to claim 2 Sayag discloses an embodiment in column 6, lines 6-15 wherein the "row logic is formed in place of two columns of the array."

In regards to claim 3 Spivey discloses that the image sensor has a thin edge around three of the sides, however this edge is about 4 pixel pitches wide (column 11, line 61 – column 12, line 5). Examiner notes that it is very well known and established in the art to make these edges as small as possible so as to increase image sensitivity when butting image sensors. Official notice is taken. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have made the edge on Spivey's image sensor to come within 2 pixel pitches instead of 4 in order to increase sensitivity of a large format array.

In regards to claim 4 see examiners notes on the rejection of claim 1.

In regards to claim 5 see examiners notes on the rejection of claim 1.

In regards to claim 6 see examiners notes on the rejection of claim 1.

In regards to claim 7 see examiners notes on the rejection of claim 3. Note that the edge around Spivey's image sensor is a guard ring.

In regards to claim 8 see examiners notes on the rejection of claims 1 and 3.

In regards to claims 9-12 see examiners notes on the rejection of claim 1.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

(USPN 5,883,830 to Hirt et al)

(USPN 6,276,605 to Olmstead et al)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian C. Genco who can be reached by phone at 703-305-7881 or by fax at 703-746-8325. The examiner can normally be reached on Monday thru Friday 8:00am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology center 2600 customer service office whose telephone number is 703-306-0377.

Brian C Genco
Examiner
Art Unit 2615

March 14, 2003

WENDY R. GARBER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600